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(54) **Temperature compensated APD detector bias and transimpedance amplifier circuitry for laser range finders**

Temperaturkompensierte Vorspannungsschaltung für einen Detektor mit Lawinenphotodiode und Transimpedenzverstärker für Laserentfernungsmesser

Circuit de polarisation pour un détecteur à photodiode à avalanche compensé en température et amplificateur d'adaptation d'impédance pour télémètres à laser

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The subject invention relates to laser range finder circuitry and, more particularly, to improved detector bias and transimpedance amplifier circuitry particularly useful with APD laser range finder receivers.

2. Description of Related Art

[0002] Prior art avalanche photodiode detectors and laser range finders incorporating such detectors are known from US-A-4464048, US-A-4001614 and DE-A-4328553.

[0003] Present laser range finder receivers rely on photodiodes for detection of target returns. There are two major categories of receiver photodiodes for detection: the acceptor intrinsic donor ("PIN") diode, and the avalanche photodiode ("APD"). Either type of device can be based on indium gallium arsenide ("InGaAs") or germanium technology. The PIN diode is the most commonly used, but requires a signal of 60 nanowatts to 100 nanowatts for a 99% probability of detection. Uncooled APD receivers currently in use are capable of 99% detection with a signal of about 10 nanowatts. Because the greater sensitivity of the APD detectors translates into a greater maximum system range, they are preferred for fabrication of a universal device applicable to a family of eye-safe laser range finders.

[0004] Current APD receivers rely on a bias network that instantaneously steps the bias voltage down by some number of volts. This instantaneous step causes the transimpedance amplifier ("TIA"), which amplifies the detector signal, to saturate. The recovery from this effect can take as long as a microsecond. The saturation condition is due to current flowing through the parasitic capacitor across the detector (approximately 1 pF) during the step voltage transition. Under these conditions a diode must be used in the TIA circuit in order to clamp the input of the TIA. This diode adds parasitic capacitance on the order of 0.8 pF, which reduces circuit sensitivity and significantly increases the cost of the detector/ preamplifier (TIA).

[0005] Present APD receivers are optimized at room temperature and, therefore, are significantly suboptimal at other operating temperatures. System sensitivity over temperature thus cannot be guaranteed. A number of components are also required for testing the frequency response of present APD amplifiers.

OBJECTS AND SUMMARY OF THE INVENTION

[0006] It is therefore an object of the invention to improve laser systems;

[0007] It is another object to improve laser range finder circuitry;

[0008] It is another object of the invention to improve detector bias and transimpedance amplifier circuitry applicable to laser range finders;

[0009] It is another object to increase sensitivity of laser range finder systems; and

[0010] It is another object to significantly improve sensitivity of laser range finder systems over temperature ranges such as -40 to +85°C while decreasing cost.

[0011] According to the present invention, there is provided a laser range finder apparatus as claimed in claim 1 hereinafter.

[0012] Thus, the net effect of the invention is lower cost and significantly higher yield due to increased margin on sensitivity, as well as optimal system performance over operating temperature extremes.

BRIEF DESCRIPTION OF THE DRAWING

[0013] The objects and features of the present invention, which are believed to be novel, are set forth with particularity in the appended claims. The present invention, both as to its organization and manner of operation, together with further objects and advantages, may best be understood by reference to the following description, taken in connection with the accompanying drawing.

[0014] FIG. 1 is an electrical circuit diagram of an APD bias circuit and transimpedance amplifier according to the preferred embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] As shown in FIG. 1, the preferred embodiment of the invention includes an APD bias circuit 311, an APD detector 315, and a transimpedance amplifier circuit 317. While the detector 315 is preferably an APD device, other detector devices, such as PINs, can be used in various embodiments according to the invention.

[0016] With respect to the APD bias circuit 311, I_{UP} and I_{DN} signals are applied to the inputs of respective inverter amplifiers A_{b1}, A_{b2}, for example, by a system microcontroller (not shown). The output of the inverter A_{b1} is applied to the gate of a first bias circuit field effect transistor (FET) Q_{b1} and to the input of a second inverter amplifier A_{b3}. The gate of the first bias circuit FET Q_{b1} is connected through a resistor R_{b1} to a reference voltage (+5 volts). The source of the first FET Q_{b1} is connected to ground, while its drain is connected to a first terminal of a resistor R_{b3}. The second terminal of the resistor R_{b3} is connected to a first terminal of a resistor R_{b2} and to the gate of a second bias circuit FET Q_{b2}. The second terminal of the resistor R_{b2} and the source of the second bias circuit FET Q_{b2} are connected in common to a 130-volt dc supply voltage. A zener diode Z_{b1} is connected in parallel with the resistor R_{b2}.

[0017] The drain of the second bias circuit FET Q_{b2} is

connected to a first terminal of a resistor R_{b4} whose second terminal is connected to the anode of a diode D_{b1} and to the drain of a third bias circuit FET Q_{b3}. The source of the third bias circuit FET Q_{b3} is connected to ground, while its gate is connected to one terminal of a resistor R_{b5} and to the output of the inverter amplifier A_{b3}. The second terminal of the resistor R_{b5} is connected to a 5-volt dc reference voltage.

[0018] The cathode of the diode D_{b1} is connected to a first terminal of a bias voltage storage capacitor C1 and to the drain of a fourth bias circuit FET Q_{b4}, whose source is grounded. The gate of the fourth bias circuit FET Q_{b4} is connected to the output of the inverter amplifier A_{b2} and to one terminal of a resistor R_{b6} whose second terminal is connected to the 5-volt dc reference voltage.

[0019] The bias voltage storage capacitor C1 has its first terminal further connected to one terminal of a resistor R1 whose second terminal is connected to a shunt capacitor C2 and to the cathode of the APD detector diode CR1. The second terminal of the capacitor C2 is grounded. The anode of the APD diode CR1 is connected to the anode of a PN diode CR3 whose cathode is further connected to ground. An AC coupling capacitor C3 connects the anode of the APD detector diode CR1 to the input of the transimpedance amplifier 317.

[0020] The input to the transimpedance amplifier 317 comprises a node constituting the intersection of the first terminals of respective resistors R4 and R5. The second terminal of the resistor R4 is connected to the gate of a first FET Q1, whose source is connected to ground and whose drain is connected to the first terminal of a resistor R12 and the emitter of an NPN transistor Q2. The second terminal of the resistor R12 is connected to one terminal of a capacitor C5 whose opposite terminal is grounded, as well as to the collector of a PNP transistor Q3.

[0021] The collector of the second transistor Q2 is connected to the anode of a PN diode CR4 and to the junction point of the second terminal of the resistor R5 and the first terminal of a resistor R6. The cathode of the PN diode CR4 is connected to one terminal of a capacitor C6 whose second terminal is connected to the base of the transistor Q2. The base of the transistor Q2 is further connected via a resistor R9 to the second terminal of the resistor R12 and to a resistor R8 whose second terminal is connected to the 5-volt dc reference voltage.

[0022] The base of the third transistor Q3 is connected to the second terminal of the resistor R5, which thus constitutes a feedback resistor from the output to the input of the amplifier 317. The emitter of the third transistor Q3 constitutes the output of the transimpedance amplifier circuit 317 and is further connected to the first terminal of a resistor R11. The second terminal of the resistor R11 is connected to the first terminal of a resistor R7, whose second terminal is connected to a -5-volt dc reference voltage. The first terminal of the resistor R7 is further connected to a first terminal of a capacitor C8 and to the second terminal of the resistor R6. The second terminal of the capacitor C8 is grounded. Examples of typical components for circuitry constructed according to the preferred embodiment are as follows:

TABLE

Resistances K(Ω)	Other Components
R_{b1} - 2	C1 - 22 nF
R_{b2} - 4.7	C2 - 10 pF
R_{b3} - 100	C3 - 15 pF
R_{b4} - 200	C5 - .01 μF
R_{b5} - 2	C6 - 10 nF
R_{b6} - 2	C8 - .01 μF
R_{b7} - 200	CR3 - HP 5082
R1 - 3.3	CR4 - HP 5082
R4 - .02	Q1 - NEC71000MVC
R5 - 51	Q2 - 2N4957
R6 - 1	Q3 - 2N2857
R7 - .01	
R8 - .01	
R9 - 1.27	
R10 - 1	
R11 - 2.3	
R12 - .160	

[0023] The foregoing values are illustrative only and may be varied in various embodiments for optimal performance in various laser range finder systems.

[0024] In operation of the circuit of FIG. 1, I_{UP} and I_{DN} control signals are selectively applied, for example, by a microcontroller. The control signal I_{UP} turns on FET Q_{b2} by turning off FET Q_{b1}, causing the gate of the FET Q_{b2} to float up in voltage. The increase in voltage permits current to flow from the 130-volt source through the resistor R_{b4} and the diode D_{b1}, causing the voltage on the bias voltage storage capacitor C1 to increase until such time as the I_{UP} control signal is turned off. The open collector type of logic gate is particularly designed to drive FETs such as FET Q_{b1}.

[0025] When the I_{UP} control signal is off, the FET Q_{b3} turns on, shorting the resistor R_{b4} to ground so as to drain off leakage current from FET Q_{b2} in order to prevent such current from further charging the capacitor C1. While I_{UP} is off, the diode D_{b1} serves to maintain the bias voltage held by the capacitor C1; i.e., it prevents discharge of the capacitor voltage by current flow through the FET Q_{b3}. The bias voltage held by the capacitor C1 may range from 30 volts to 90 volts and is determined by the length of time I_{UP} is "on" and the breakdown voltage of the APD 315.

[0026] Application of the I_{DN} control signal turns on the FET Q_{b4} and discharges the bias voltage storage capacitor C1 to ground through the resistor R_{b7}. Both I_{UP} and I_{DN} are off when the circuitry is inactive.

[0027] Once the bias voltage storage capacitor C1 has been charged, the detector circuit 315 is biased for operation, for example, to detect a laser pulse return after firing of a laser. When the laser is initially fired, a large amount of energy is reflected or "back-scattered" back into the laser range finder optics, causing the TIA amplifier 317 to saturate. Accordingly, the diode CR3 is employed in the circuit to become forward biased by the increase in detector voltage and to dump the charge to ground; i.e., the diode CR3 comprises protection circuitry for accommodating initial overloads. The circuit provided by the capacitor C2 and the resistor R1 connected to the APD 315 limits the amount of energy which can be dumped through the diode CR3. After the diode CR3 stops conducting, the voltage on the capacitor C2 rapidly increases, via charging current flow through the capacitor C1 and the resistor R1.

[0028] The capacitor C3 is an AC coupling capacitor, which connects the detector circuit to the TIA 317. The TIA 317 itself may be viewed as a typical operational amplifier having a feedback resistor R5 connected between its output and inverting input which, in an illustrative embodiment, has a value of 51 KΩ.

[0029] In the preferred TIA amplifier 317 shown in FIG. 1, the current flowing into the R4-R5-C3 node is multiplied by the value of the feedback resistor R5, producing an output voltage at the emitter of the third transistor Q3. The FET Q1 has a "gm" parameter associated with it, which is basically a voltage-to-current converting factor. As current flows through the coupling capacitor C3, the gate voltage on the FET Q1 rises, causing more current flow through the FET Q1. The transistor Q2 tries to hold the drain of the FET Q1 at a constant voltage. Thus, as the FET Q1 "asks" for more current, the transistor Q2 turns off. As the transistor Q2 shuts off, in order to hold steady state, its collector voltage moves down, producing a voltage across the feedback resistor R5. For the selected value of R5 of 51 KΩ, this voltage ultimately equals 51 KΩ times the current flowing through the AC coupling capacitor C3. The transistor Q3 is a buffer-follower whose emitter voltage side is .7 below the voltage on its base (i.e., the voltage developed across the feedback resistor R5).

[0030] The TIA amplifier resistor R6 can be used to achieve a manufacturing advantage according to the preferred embodiment. The stability of the amplifier is a function of the open loop gain, which is determined by the "gm" of the FET Q1 and the value of the resistor R6. Thus, if gm changes, the value of R6 may be adjusted to compensate for it. Thus, in production, an entire wafer of FETs Q1 may be fabricated. After R6 is adjusted to get proper compensation for one of the FETs Q1 from the wafer, all devices on that wafer can be used with the same R6 value.

[0031] As to the remainder of the components, resistors R9 and R10 bias the transistor Q2 and set its operating point. The capacitor C6 makes the node an AC short circuit. The diode CR4 prevents circuit overload. The resistors R7 and R11 are respectively used for power supply isolation and to bias the second transistor Q3.

[0032] The feedback resistor R5 determines the amount of transimpedance gain, i.e., current-to-voltage transfer. Whatever current goes through C3 x 51K equals the output voltage swing. The feedback resistor R5 further determines the ultimate bandwidth of the system. Lowering the value of R5 provides more bandwidth, enabling the system to operate with shorter laser pulses.

[0033] The detector 315 and TIA amplifier 317 are preferably formed as a hybrid circuit on a common substrate such as alumina.. A temperature sensor 319 is mounted on the substrate next to the detector 315 and enables optimizing the receiver as a function of temperature. Thus, an associated microcontroller may continuously monitor and recalibrate the receiver as a function of temperature. The temperature sensor 319 may be a commercially available AD590 sensor wherein a reference voltage is applied to a first terminal +TS, producing a current at a second terminal -TS which is related to temperature. This current is converted to a voltage which enables an associated microcontroller to read the temperature of the detector 315.

[0034] The frequency response of the system of FIG. 1 is measured by illuminating the detector 315 with an unmodulated CW source and looking at the noise spectrum at the output TIA OUT of the amplifier 317. The noise spectrum will have a power envelope versus frequency that is characteristic of the detector/preamplifier frequency response. The frequency response of the amplifier will vary from part to part due to the "gm" parameter of the preferred NEC71000 GaAs FET. The feedback loop can compensate for this effect by adjusting the values of the resistors R5 and R6. This is an important cost savings because the select-in-test only occurs once for each lot-buy of the NEC71000 FET. Therefore, the value of the resistor R6 is selected on the first unit and is fixed for the balance of the production run. The value of the resistor R5 is not normally changed because it affects the amount of output voltage.

[0035] Another feature of this design is the addition of the temperature sensor 319 within the detector/preamplifier package. The optimum detector bias voltage can shift dramatically with temperature changes. The temperature sensor 319 allows the system to monitor this condition and self-calibrate the receiver operating parameters, such as receiver offset voltages, false alarm rate, and APD bias voltage. Essentially, the receiver can be optimized for performance over the entire operating temperature range.

[0036] The receiver sensitivity is optimized by increasing the APD bias voltage (this increases the APD gain) until the APD noise is larger than the electronics noise. Once the APD noise begins to dominate the electronics noise of the preamplifier 317, further increases in APD gain will reduce the system NEP (noise equivalent power). At low temperatures, the APD gain must be high in order to overcome the preamplifier noise. This is

due to low leakage currents within the APD at low temperatures. Under these conditions, the APD noise may not be larger than the preamplifier noise because of limitations in achievable APD gain. All of these effects can be optimized by monitoring the APD temperature along with self-calibrating electronics.

[0037] Those skilled in the art will appreciate that various adaptations and modifications of the just-described preferred embodiment can be configured without departing from the scope of the invention. Therefore, it is to be understood that, within the scope of the appended claims, the invention may be practiced other than as specifically described herein.

Claims

1. Laser range finder apparatus comprising:

   a photodiode detector (315) having a first terminal and a second output terminal;
   a charge storage device (C1) connected to the first terminal of said photodiode detector (315) for storing a detector bias voltage;
   a first circuit including a transistor switch (Q_{b4}) connected to said charge storage device and responsive to a first control signal to discharge said charge storage device (C1);
   a second circuit for charging said charge storage device;

   characterised in that:

   said second circuit comprises a current source (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}), connected to said charge storage device, responsive to a second control signal to apply a charging current to said charge storage device such that said detector bias voltage is determined by the duration of said second control signal; and
   the laser range finder further includes a temperature sensing circuit (319) mounted in the vicinity of said photodiode detector (CR1) for monitoring the temperature in said vicinity and providing a signal indicative thereof.

2. The laser range finder apparatus of Claim 1 further including a transimpedance amplifier (317) having an input connected to said second output terminal and an output.

3. The laser range finder apparatus of Claim 1 wherein said current source (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}) includes a first field effect transistor (Q_{b2}) having a first terminal connected to a voltage source, said field effect transistor (Q_{b2}) being switchable to cause supply of said charging current to said charge storage device (C1).

4. The laser range finder apparatus of Claim 3 wherein said current source (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}) includes a second field effect transistor having a gate terminal connected to receive said second control signal and a first terminal connected through a resistance (R_{b3}) to the gate of said first field effect transistor (Q_{b2}).

5. The laser range finder apparatus of Claim 4 further including a third field effect transistor (Q_{b3}) having a gate, an inverter (A_{b3}) having an output connected to said gate, said inverter having an input connected to receive said second control signal, said third field effect transistor (Q_{b3}) further having a first terminal connected to the anode of a diode (D_{b1}) and a second terminal connected to ground, said diode (D_{b1}) further having a cathode connected to said charge storage device (C1).

6. The laser range finder apparatus of Claim 1 further including an overload protection circuit including a diode (CR3) connected to said photodiode detector (CR1) and to ground.

7. The laser range finder apparatus of Claim 1 wherein said overload protection circuit further includes a resistor-capacitor network (R1, C2) having a connection to said photodiode detector (CR1) for limiting the amount of excess charge which can be dumped through said diode (CR3).

8. The laser range finder apparatus of Claim 2 wherein said transimpedance amplifier (317) applies a current-to-voltage transfer factor to a current at its input so as to produce a voltage at its output which is a multiple of said current.

9. The laser range finder apparatus of Claim 8 wherein said transimpedance amplifier (317) includes a field effect transistor (Q1) and a first resistance (R6) and has an open loop gain determined by a parameter "gm" of said field effect transistor (Q1) and by the value of said first resistance (R6); and wherein the value of said first resistance (R6) is adjusted to compensate for variations in the parameter "gm" in order to maintain a desired open loop gain.

10. The laser range finder apparatus of Claim 8 wherein said transimpedance amplifier 317 further includes a feedback resistance (R5) whose value is said multiple.

11. The laser range finder apparatus of Claim 8 wherein said feedback resistance (R5) is adjustable to increase the bandwidth of said apparatus.

12. The laser range finder apparatus of Claim 1 wherein said photodiode detector (CR1) comprises an ava-

lanche photodiode.

Patentansprüche

1. Laserentfernungsmeßvorrichtung mit:

   einem Photodiodendetektor (315), der einen ersten Anschluß und einen zweiten Ausgangsanschluß aufweist;

   einer Ladungsspeichervorrichtung (C1), die mit dem ersten Anschluß des Photodiodendetektors (315) zum Speichern einer Detektorvorspannung verbunden ist;

   einer ersten Schaltung, die einen Transistorschalter (Q_{b4}) aufweist, der mit der Ladungsspeichervorrichtung verbunden ist und auf ein erstes Steuersignal anspricht, um die Ladungsspeichervorrichtung (C1) zu entladen;

   einer zweiten Schaltung zum Laden der Ladungsspeichervorrichtung;

   dadurch gekennzeichnet, daß

   die zweite Schaltung eine Stromquelle (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}) aufweist, die mit der Ladungsspeichervorrichtung verbunden ist, auf ein zweites Steuersignal anspricht, um einen Ladestrom der Ladungsspeichervorrichtung zuzuführen, so daß die Detektorvorspannung durch die Dauer des zweiten Steuersignals bestimmt wird; und

   der Laserentfernungsmesser ferner eine Temperaturerfassungsschaltung (319) aufweist, die in der Nähe des Photodiodendetektors (CR1) angebracht ist, um die Temperatur in dieser Umgebung zu überwachen und ein die Temperatur anzeigendes Signal zu liefern.

2. Laserentfernungsmeßvorrichtung nach Anspruch 1, ferner mit einem Transimpedanzverstärker (317), der einen Eingang, der mit dem zweiten Ausgangsanschluß verbunden ist, und einen Ausgang aufweist.

3. Laserentfernungsmeßvorrichtung nach Anspruch 1, wobei die Stromquelle (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}) einen ersten Feldeffekttransistor (Q_{b2}) aufweist, der einen ersten mit einer Spannungsquelle verbundenen Anschluß aufweist, wobei der Feldeffekttransistor (Q_{b2}) schaltbar ist, um den Ladestrom der Ladungsspeichervorrichtung (C1) zuzuführen.

4. Laserentfernungsmeßvorrichtung nach Anspruch 3, wobei die Stromquelle (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}) einen zweiten Feldeffekttransistor aufweist, der einen Gate-Anschluß, der zum Empfang des zweiten Steuersignals verbunden ist, und einen ersten Anschluß aufweist, der über einen Widerstand (R_{b3}) mit dem Gate des ersten Feldeffekttransistors (Q_{b2}) verbunden ist.

5. Laserentfernungsmeßvorrichtung nach Anspruch 4, ferner mit einem dritten Feldeffekttransistor (Q_{b3}), der ein Gate aufweist, wobei ein Inverter (A_{b3}) einen mit dem Gate verbundenen Ausgang aufweist, wobei der Inverter einen Eingang besitzt, der verbunden ist, um das zweite Steuersignal zu empfangen, wobei der dritte Feldeffekttransistor (Q_{b3}) ferner einen ersten mit der Anode der Diode (D_{b1}) verbundenen Anschluß und einen mit Masse verbundenen zweiten Anschluß aufweist, wobei die Diode (D_{b1}) ferner eine Kathode aufweist, die mit der Ladungsspeichervorrichtung (C1) verbunden ist.

6. Laserentfernungsmeßvorrichtung nach Anspruch 1, ferner mit einer Überlastschutzschaltung, die eine Diode (CR3) aufweist, die mit dem Photodiodendetektor (CR1) und Masse verbunden ist.

7. Laserentfernungsmeßvorrichtung nach Anspruch 1, wobei die Überlastschutzschaltung ferner ein Widerstands-Kondensatornetzwerk (R1, C2) aufweist, das eine Verbindung zu dem Photodiodendetektor (CR1) hat, um den Betrag der überschüssigen Ladung zu begrenzen, die durch die Diode (CR3) entladen werden kann.

8. Laserentfernungsmeßvorrichtung nach Anspruch 2, wobei der Transimpedanzverstärker (317) an seinem Eingang auf einen Strom einen Strom-zu-Spannungs-Übertragungsfaktor anwendet, um eine Spannung an seinem Ausgang zu produzieren, die ein Vielfaches des Stroms ist.

9. Laserentfernungsmeßvorrichtung nach Anspruch 8, wobei der Transimpedanzverstärker (317) einen Feldeffekttransistor (Q1) und einen ersten Widerstand (R6) aufweist und eine Leerlaufverstärkung besitzt, die durch einen Parameter "gm" des Feldeffekttransistors (Q1) bestimmt ist und durch einen Wert des ersten Widerstands (R6); und wobei der Wert des ersten Widerstands (R6) eingestellt wird, um Variationen des Parameters "gm" zu kompensieren, um eine gewünschte Leerlaufverstärkung aufrechtzuerhalten.

10. Laserentfernungsmeßvorrichtung nach Anspruch 8, wobei der Transimpedanzverstärker (317) ferner einen Rückkopplungswiderstand (R5) besitzt, des-

sen Wert das Vielfache ist.

11. Laserentfernungsmeßvorrichtung nach Anspruch 8, wobei der Rückkopplungswiderstand (R5) einstellbar ist, um die Bandbreite der Vorrichtung zu erhöhen.

12. Laserentfernungsmeßvorrichtung nach Anspruch 1, wobei der Photodiodendetektor (CR1) eine Lawinenphotodiode aufweist.

Revendications

1. Dispositif télémètre à laser, comprenant :

un détecteur à photodiode (315) comportant une première borne et une seconde borne de sortie ;
un dispositif d'accumulation de charge (C1) connecté à la première borne dudit détecteur à photodiode (315) destiné à accumuler une tension de polarisation de détecteur ;
un premier circuit incluant un commutateur à transistor (Q_{b4}) connecté audit dispositif d'accumulation de charge et sensible à un premier signal de commande pour décharger ledit dispositif d'accumulation de charge (C1) ;
un second circuit destiné à charger ledit dispositif d'accumulation de charge ;

caractérisé en ce que :

ledit second circuit comprend une source de courant (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}), connectée audit dispositif d'accumulation de charge, sensible à un second signal de commande pour appliquer un courant de charge audit dispositif d'accumulation de charge de sorte que ladite tension de polarisation de détecteur est déterminée par la durée dudit second signal de commande ; et
le télémètre à laser comprend en outre un circuit de détection de température (319) monté à proximité dudit détecteur à photodiode (CR1) pour surveiller la température dans ledit voisinage et fournir un signal indicatif de celle-ci.

2. Dispositif télémètre à laser selon la revendication 1, incluant en outre un amplificateur d'adaptation d'impédance (317) comportant une entrée connectée à ladite seconde borne de sortie et une sortie.

3. Dispositif télémètre à laser selon la revendication 1, dans lequel ladite source de courant (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}) inclut un premier transistor à effet de champ (Q_{b2}) comportant une première borne connectée à une source de tension, ledit transistor à effet de champ (Q_{b2}) pouvant commuter pour provoquer l'application dudit courant de charge audit dispositif d'accumulation de charge (C1).

4. Dispositif télémètre à laser selon la revendication 3, dans lequel ladite source de courant (R_{b1}, Q_{b1}, R_{b3}, R_{b2}, Z_{b1}, Q_{b2}, R_{b4}) inclut un deuxième transistor à effet de champ comportant une borne de grille connectée pour recevoir ledit second signal de commande et une première borne connectée, par l'intermédiaire d'une résistance (R_{b3}), à la grille dudit premier transistor à effet de champ (Q_{b2}).

5. Dispositif télémètre à laser selon la revendication 4, incluant en outre un troisième transistor à effet de champ (Q_{b3}) comportant une grille, un inverseur (A_{b3}) comportant une sortie connectée à ladite grille, ledit inverseur comportant une entrée connectée pour recevoir ledit second signal de commande, ledit troisième transistor à effet de champ (Q_{b3}) comportant en outre une première borne connectée à l'anode d'une diode (D_{b1}) et une seconde borne connectée à la masse, ladite diode (D_{b1}) comportant en outre une cathode connectée audit dispositif d'accumulation de charge (C1).

6. Dispositif télémètre à laser selon la revendication 1, incluant en outre un circuit de protection contre les surcharges incluant une diode (CR3) connectée audit détecteur à photodiode (CR1) et à la masse.

7. Dispositif télémètre à laser selon la revendication 1, dans lequel ledit circuit de protection contre les surcharges comprend en outre un réseau de résistance - capacité (R1, C2) comportant une connexion audit détecteur à photodiode (CR1) pour limiter la quantité de charge en excès qui peut être évacuée par ladite diode (CR3).

8. Dispositif télémètre à laser selon la revendication 2, dans lequel ledit amplificateur d'adaptation d'impédance (317) applique, au niveau de son entrée, un facteur de transfert d'intensité à tension à un courant, de façon à produire, au niveau de sa sortie, une tension qui est un multiple de ladite intensité.

9. Dispositif télémètre à laser selon la revendication 8, dans lequel ledit amplificateur d'adaptation d'impédance (317) inclut un transistor à effet de champ (Q1) et une première résistance (R6), et a un gain en boucle ouverte déterminé par un paramètre " gm " dudit transistor à effet de champ (Q1) et par la valeur de ladite première résistance (R6) ; et dans lequel la valeur de ladite première résistance (R6) est réglée pour compenser des variations du paramètre " gm " afin de maintenir un gain en boucle ouverte souhaité.

10. Dispositif télémètre à laser selon la revendication 8, dans lequel ledit amplificateur d'adaptation d'impédance (317) comprend en outre une résistance de contre-réaction (R5) dont la valeur est ledit multiple.

11. Dispositif télémètre à laser selon la revendication 8, dans lequel ladite résistance de contre-réaction (R5) peut être réglée pour augmenter la largeur de bande dudit dispositif.

12. Dispositif télémètre à laser selon la revendication 1, dans lequel ledit détecteur à photodiode (CR1) comprend une photodiode à avalanche.

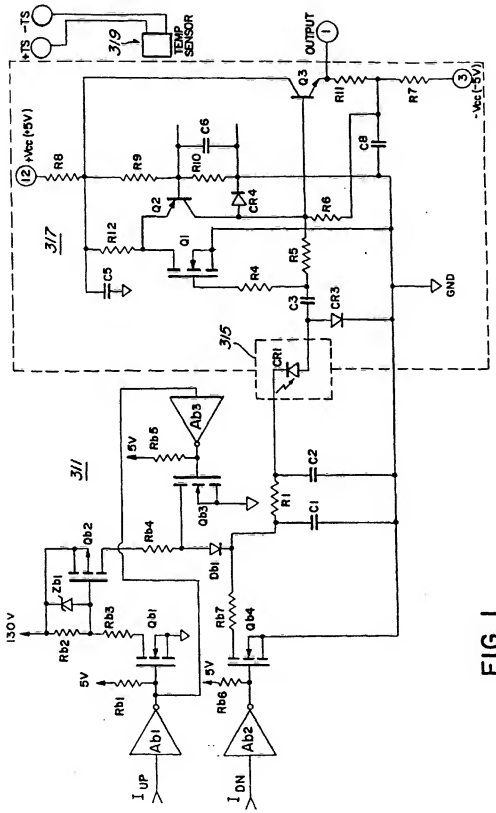
+TS
-TS
319
TEMP SENSOR
OUTPUT
Q3
R11
R7
-Vcc (-5V)
+Vcc (+5V)
R8
R9
R10
C6
C8
Q2
CR4
R6
317
R12
Q1
C5
R5
R4
C3
CR3
GND
315
CR1
311
Ab3
5V
Rb5
Qb3
C2
R1
C1
Qb2
Rb4
Db1
Zb1
130V
Rb2
Rb3
Qb1
Rb7
Qb4
5V
Rb1
5V
Rb6
Ab1
Ab2
I UP
I DN

FIG. 1

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
GARY S. WILLIAMS
PENNIE & EDMONDS LLP
1155 AVENUE OF THE AMERICAS
NEW YORK, NY 10036

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT OR THE DECLARATION

(PCT Rule 44.1).

	Date of Mailing (*day/month/year*)
Applicant's or agent's file reference 9775-052-228	FOR FURTHER ACTION See paragraphs 1 and 4 below
International application No. PCT/US02/03226	International filing date (*day/month/year*) 04 February 2002 (04.02.2002)
Applicant FINISAR CORPORATION	

1. ☒ The applicant is hereby notified that the international search report has been established and is transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34, chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: (41-22) 740.14.35

   For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect is transmitted herewith.

3. ☐ With regard to the protest against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. Reminders

   Shortly after **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90 *bis*.1 and 90 *bis*.3, respectively, before the completion of the technical preparations for international publication.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase until **30 months** from the priority date (in some Offices even later); otherwise the applicant must, within **20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US Commissioner for Patents Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Jason Chan Telephone No. 703-305-4700

Form PCT/ISA/220 (April 2002) (*See notes on accompanying sheet*)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 9775-052-228	**FOR FURTHER ACTION**	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
International application No. PCT/US02/03226	International filing date (*day/month/year*) 04 February 2002 (04.02.2002)	(Earliest) Priority Date (*day/month/year*) 05 February 2001 (05.02.2001)
Applicant FINISAR CORPORATION		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☒ It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the Report
   a. With regard to the language, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.
   ☐ the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).
   b. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, the international search was carried out on the basis of the sequence listing:
   ☐ contained in the international application in written form.
   ☐ filed together with the international application in computer readable form.
   ☐ furnished subsequently to this Authority in written form.
   ☐ furnished subsequently to this Authority in computer readable form.
   ☐ the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   ☐ the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.
2. ☐ Certain claims were found unsearchable (See Box I).
3. ☐ Unity of invention is lacking (See Box II).
4. With regard to the title,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the abstract,
   ☐ the text is approved as submitted by the applicant.
   ☒ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. The figure of the drawings to be published with the abstract is Figure No. 3
   ☒ as suggested by the applicant.
   ☐ because the applicant failed to suggest a figure.
   ☐ because this figure better characterizes the invention.
   ☐ None of the figures

Form PCT/ISA/210 (first sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/03226

Box III TEXT OF THE ABSTRACT (Continuation of Item 5 of the first sheet)

The technical features mentioned in the abstract do not include a reference sign between parentheses (PCT Rule 8.1(d)).

NEW ABSTRACT

A controller (110) for controlling a transceiver having a laser transmitter and a photodiode receiver. The controller includes memory (120, 122, 128) for storing information related to the transceiver, and analog to digital conversion circuitry (127) for receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory. Comparison logic (131) compares one or more of these digital values with limit values, generates flag values based on the comparisons, and stores the flag values in predefined locations within the memory. Control circuitry (123-1, 123-2) in the controller controls the operation of the laser transmitter in accordance with one or more values stored in the memory. A serial interface (121) is provided to enable a host device to read from and write to locations within the memory. Excluding a small number of binary input and output signals, all control and monitoring functions of the transceiver are mapped to unique memory mapped locations within the controller. A plurality of the control functions and a plurality of the monitoring functions of the controller are exercised by a host computer by accessing corresponding memory mapped locations within the controller.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/03226

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H04B 10/00
US CL. : 359/152
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 359/110, 152, 180, 187; 257/80

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,057,932 A (LANG) 15 October 1991 (15.10.1991), Figures 2 and 3.	1-19
Y	US 6,023,147 A (CARGIN, Jr. et al.) 08 February 2000 (08.02.2000), columns 22 and 23.	1-19
Y	US 6,010,538 A (SUN et al.) 04 January 2000 (04.01.2000), Figure 10.	1-19
Y	US 6,115,113 A (FLOCKENCIER) 05 September 2000 (05.09.2000), Figure 3 and columns 6-8.	1-19
Y	US 5,943,152 A (MIZRAHI et al.) 24 August 1999 (24.08.1999), entire document.	4-6, 13-15
Y	US 6,012,947 A (SWARTZ) 08 February 2000 (08.02.2000), entire document.	1-19
Y	US H1,881 H (DAVIS et al.) 03 October 2000 (03.10.2000), Figure 8.	1-19
Y	US 4,545,078 A (WIEDEBURG) 01 October 1985 (01.10.1985), Figure 2.	1-19

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 April 2002 (15.04.2002)	09 MAY 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Jason Chan Telephone No. (703) 305-4700

Form PCT/ISA/210 (second sheet) (July 1998)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

CA

PCT

To:
GARY S. WILLIAMS
PENNIE & EDMONDS LLP
1155 AVENUE OF THE AMERICAS
NEW YORK, NY 10036

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference 9775-052-228	Date of Mailing *(day/month/year)* FOR FURTHER ACTION See paragraphs 1 and 4 below
International application No. PCT/US02/03226	International filing date *(day/month/year)* 04 February 2002 (04.02.2002)
Applicant FINISAR CORPORATION	

1. ☒ The applicant is hereby notified that the international search report has been established and is transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34, chemin des Colombettes
   1211 Geneva 20, Switzerland, Facsimile No.: (41-22) 740.14.35

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Name and mailing address of the ISA/US Commissioner for Patents Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Jason Chan Telephone No. 703-305-4700

Form PCT/ISA/220 (April 2002) *(See notes on accompanying sheet)*

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
GARY S. WILLIAMS
PENNIE & EDMONDS LLP
1155 AVENUE OF THE AMERICAS
NEW YORK, NY 10036

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT OR THE DECLARATION

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Applicant's or agent's file reference 9775-052-228	Date of Mailing (day/month/year) FOR FURTHER ACTION See paragraphs 1 and 4 below
International application No. PCT/US02/03226	International filing date (day/month/year) 04 February 2002 (04.02.2002)
Applicant FINISAR CORPORATION	

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   Where? Directly to the International Bureau of WIPO, 34, chemin des Colombettes
   1211 Geneva 20, Switzerland, Facsimile No.: (41-22) 740.14.35

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Name and mailing address of the ISA/US Commissioner for Patents Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Jason Chan Telephone No. 703-305-4700

Form PCT/ISA/220 (April 2002) *(See notes on accompanying sheet)*

NOTES TO FORM PCT/ISA/220 (continued)

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33 and 36 unchanged; new claims 49 to 51 added."
2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."
3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."
4. [Where various kinds of amendments are made]:
"Claims 1-10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under Article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

The statement should be brief, it should not exceed 500 words if in English or if translated into English.

It should not be confounded with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It should not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

In what language ?

The amendments must be made in the language in which the international application is published. The letter and any statement accompanying the amendments must be in the same language as the international application if that language is English or French; otherwise, it must be in English or French, at the choice of the applicant.

Consequence if a demand for international preliminary examination has already been filed ?

If, at the time of filing any amendments under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the same time of filing the amendments with the International Bureau, also file a copy of such amendments with the International Preliminary Examining Authority (see Rule 62.2(a), first sentence).

Consequence with regard to translation of the international application for entry into the national phase ?

The applicant's attention is drawn to the fact that, where upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see Volume II of the PCT Applicant's Guide.